What is claimed is:

1. A parallel execution processor comprising:

a plurality of processing elements;

an obtaining unit operable to obtain (i) a piece of group number information indicating how many groups the processing elements should be formed into and (ii) an instruction sequence including one or more instructions;

a decoding unit operable to decode the obtained instruction sequence;

a group forming unit operable to form the processing elements into as many groups as indicated by the piece of group number information; and

an execution controlling unit operable to assign part or all of the instructions included in the decoded instruction sequence to the groups, so that one group receives one instruction, and control the processing elements so that (i) the instructions received by the groups are executed in parallel, and (ii) in each group, all processing elements in the group are employed in parallel for the execution of the received instruction.

2. The parallel execution processor of Claim 1, wherein

the instruction sequence includes as many instructions as the number of groups indicated by the piece of group number

information.

3. The parallel execution processor of Claim 2, wherein

the number of groups indicated by the piece of group number information is either one or two,

when the number of groups indicated is one, the group forming unit forms all of the processing elements into one group, and

when the number of groups indicated is two, the group forming unit forms all of the processing elements into two groups so that the two groups contain an equal number of processing elements.

4. The parallel execution processor of Claim 3, further comprising

a register that includes a plurality of register files each of which corresponds to a different one of the processing elements, wherein

the instruction sequence includes a first instruction and a second instruction,

the register files are arranged in the register so that first-group register files and second-group register files alternate, (i) the first-group register files each storing therein a piece of data to be processed when the first instruction

is executed and (ii) the second-group register files each storing therein a piece of data to be processed when the second instruction is executed,

when the number of groups indicated is two, the group forming unit forms the processing elements corresponding to the first-group register files into one of the two groups, and the processing elements corresponding to the second-group register files into the other group, and

each of the processing elements obtains the piece of data to be processed from the corresponding register file.

5. The parallel execution processor of Claim 4, wherein

the register files are formed into a plurality of pairs, keeping an order in which the register files are arranged in the register,

each of the instructions includes a piece of selection information indicating which piece of data, each processing element should obtain, selecting out of (a) the piece of data stored in the corresponding register file and (b) the piece of data stored in a register file with which the corresponding register file is paired, and

each of the processing elements obtains the piece of data to be processed from the register file indicated in each piece of selection information.

6. The parallel execution processor of Claim 3, wherein when the number of groups indicated is two, the execution controlling unit includes:

a storing unit that stores therein a plurality of combination options based on which of the processing elements should belong to each of the two groups, the combination options being prepared for each of a plurality of grouping procedures;

a grouping information obtaining unit operable to obtain a piece of grouping information indicating which one of the grouping procedures should be used; and

a selecting unit operable to select one of the combination options according to the obtained piece of grouping information.

7. The parallel execution processor of Claim 3, wherein when the number of groups indicated is two, the execution controlling unit includes:

a grouping information obtaining unit operable to obtain a piece of grouping information indicating to which one of the two groups, each of the processing elements should belong; and

a grouping unit operable to form the processing elements into the two groups according to the obtained piece of grouping information.

8. The parallel execution processor of Claim 1, further comprising

a fetching unit operable to fetch a piece of data which is of a predetermined length and has a format field and a data field, wherein

each of the instructions includes an OP code and an operand,

a positioning pattern is written in the format field, the positioning pattern being for positioning OP codes and operands in the data field,

in the piece of data, one or more OP codes and one or more operands are arranged in the data field in an order defined by the positioning pattern written in the format field,

the number of groups indicated by the piece of group number information is a number of instructions defined by the positioning pattern,

the decoding unit extracts, from the piece of data, the one or more OP codes and the one or more operands, according to the positioning pattern so as to decode the OP codes and the operands of the instructions, and

the execution controlling unit assigns, in the defined order, the decoded instructions to the groups.

9. The parallel execution processor of Claim 1, further comprising:

a fetching unit operable to fetch a piece of data which is of a predetermined length; and

a storing unit operable to store therein a predetermined positioning pattern for OP codes and operands, wherein

each of the instructions includes an OP code and an operand,

one or more OP codes and one or more operands are arranged in the piece of data in an order defined by the predetermined positioning pattern,

the number of groups indicated by the piece of group number information is a number of instructions defined by the positioning pattern,

the decoding unit extracts, from the piece of data, the one or more OP codes and the one or more operands, according to the positioning pattern so as to decode the OP codes and the operands of the instructions, and

the execution controlling unit assigns, in the defined order, the decoded instructions to the groups.

10. The parallel execution processor of Claim 1, wherein

when the number of groups indicated by the piece of group number information is two or larger, the obtaining unit obtains an instruction that instructs that processing elements included in some of the groups should halt operation, and

the execution controlling unit controls the processing

elements included in those groups so that those processing elements halt operation.

11. A parallel execution processor comprising:

a plurality of processing elements;

a register that includes a plurality of register files each of which corresponds to a different one of the processing elements, the register files being arranged in the register so that first-group register files and second-group register files are positioned according to a predetermined rule, (i) the first-group register files each storing therein a piece of data to be processed when a first instruction is executed and (ii) the second-group register files each storing therein a piece of data to be processed when a second instruction is executed;

an obtaining unit operable to obtain an instruction sequence that includes the first instruction and the second instruction;

a decoding unit operable to decode the first instruction and the second instruction included in the obtained instruction sequence; and

an execution controlling unit operable to assign (i) the first instruction to the processing elements corresponding to the first-group register files and (ii) the second instruction to the processing elements corresponding to the second-group

register files and control the processing elements so that (i) the first and second instructions are executed in parallel, (ii) the processing elements executing the first instruction are employed in parallel for the execution, and (iii) the processing elements executing the second instruction are employed in parallel for the execution.

12. The parallel execution processor of Claim 11, wherein

the register files are arranged in the register so that the first-group register files and the second-group register files alternate.

13. The parallel execution processor of Claim 12, wherein

the register files are formed into a plurality of pairs, keeping an order in which the register files are arranged in the register,

each of the instructions includes a piece of selection information indicating which piece of data, each processing element should obtain, selecting out of (a) the piece of data stored in the corresponding register file and (b) the piece of data stored in a register file with which the corresponding register file is paired, and

each of the processing elements obtains the piece of data to be processed from the register file indicated in each piece

of selection information.

14. An instruction assigning method for assigning instructions to a plurality of processing elements, comprising:

an obtaining step of obtaining (i) a piece of group number information indicating how many groups the processing elements should be formed into and (ii) an instruction sequence including one or more instructions;

a decoding step of decoding the obtained instruction sequence;

a group forming step of forming the processing elements into as many groups as indicated by the piece of group number information; and

an execution controlling step of assigning part or all of the instructions included in the decoded instruction sequence to the groups, so that one group receives one instruction, and controlling the processing elements so that (i) the instructions received by the groups are executed in parallel, and (ii) in each group, all processing elements in the group are employed in parallel for the execution of the received instruction.

15. An instruction assigning method for assigning a first instruction and a second instruction to a plurality of processing elements, the instruction assigning method

comprising:

a storing step of (i) reading as many pieces of data as the number of processing elements, from a memory in which (a) pieces of data to be processed when a first instruction is executed and (b) piece of data to be processed when a second instruction is executed are arranged in an order according to a predetermined rule and (ii) storing the pieces of data, without changing the order, into register files each of which corresponds to a different one of the processing elements;

an obtaining step of obtaining an instruction sequence that includes the first instruction and the second instruction;

a decoding step of decoding the first instruction and the second instruction included in the obtained instruction sequence; and

an execution controlling step of assigning (i) the first instruction to the processing elements corresponding to the register files that each store therein the piece of data to be processed when the first instruction is executed and (ii) the second instruction to the processing elements corresponding to the register files that each store therein the piece of data to be processed when the second instruction is executed, and controlling the processing elements so that (i) the first and the second instructions are executed in parallel, (ii) the processing elements executing the first instruction are employed

in parallel for the execution, and (iii) the processing elements executing the second instruction are employed in parallel for the execution.